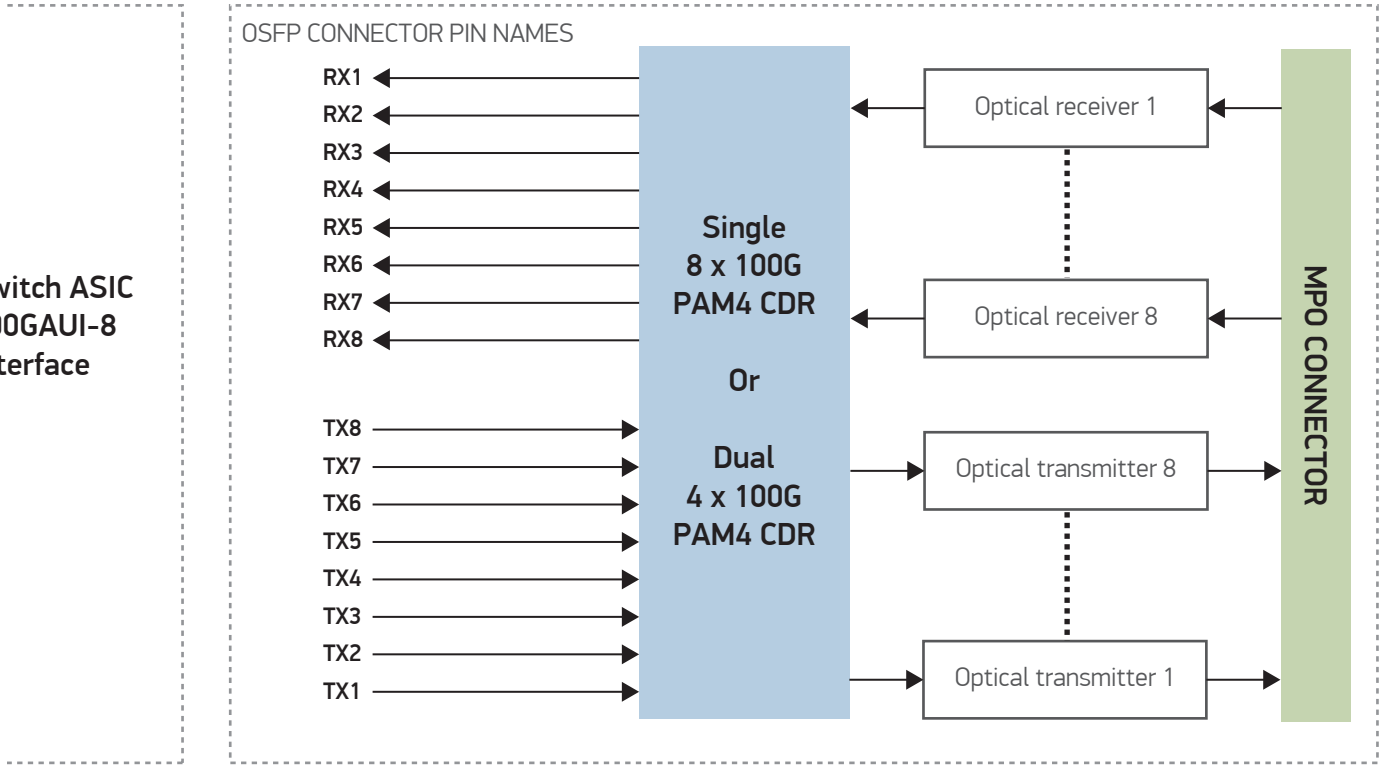
800G OSFP-2xDR4 500m Transceiver

ET8001-2DR4

Based on a 5nm DSP and cooled 1310 EML laser technology, the ET8001-2DR4 is an 800G 2 x DR4 OSFP transceiver module compliant with the 800 Gigabit hot-pluggable OSFP Multi-Source Agreement (MSA) used for up to 8 x 100G PAM4 data rates over 500 m single mode fiber.

Optical PMD Illustration



Product Features

- Hot-pluggable OSFP form factor
- Compliant with IEEE Std 802.3cu 400GBASE-DR4
- Electrical interface compliant with 100Gbps per lane defined by IEEE 802.3ck
- 8 x 100G PAM4/8 x 50G PAM4 data rates
- OSFP MSA package with dual APC MPO-12 connectors
- 5nm DSP for low power dissipation: <14W
- Cooled 1310 EML laser
- I^2C management interface compliant to CMIS Rev5.0 with integrated Digital Diagnostics Monitoring
- Control interface compliant with OSFP MSA
- Internal CDR on both transmitter and receiver channels
- Up to 500 m on 9/125um SMF
- Single 3.3 V power supply
- Class 1 laser safety certified
- Operating case temperature range: 0°C to 70 °C
- RoHS6 compliant

Applications

- High-speed Ethernet networks
- 2 x 400G-DR4 applications
- 2 x 200G-DR4 applications

Ordering Information

Model Name	Transmitter	Output Power OMA[1] @106.25G	Receiver	Reach	OMA Sensitivity[2] @106.25G	Case Temp.	DDMI	CMIS
ET8001-2DR4	Cooled EML	-0.8 ~ +4.2dBm	PIN	500m	<-3.9dBm	0~70°C	Yes	CMIS5.0

Notes:

1. Refer to Transmitter Optical Characteristics details.
2. Refer to Receiver Optical Characteristics details

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Parameter	Symbol	Min.	Max.	Unit
Storage Temperature	T_S	-40	85	°C
Relative Humidity	RH	5	95	%
Supply Voltage	V_{CC}	-0.5	3.6	V

Recommended Operating Conditions

Parameter	Symbol	Min.	Typical	Max.	Unit
Operating Case Temperature	T_C	0	-	70	°C
Supply Voltage	V_{CC}	3.135	3.3	3.465	V
Data Rate per Channel		-	53.125	V	%
		-	26.2525	-	GBd
Modulation Format			PAM4		GBd

Transceiver Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Power Dissipation	P_D	-	-	14	W	
Input Differential Impedance	Z_{IN}	90	100	110	Ω	-
Differential Data Input Swing	$V_{IN, P-P}$	-	-	900	mVP-P	-
DC Common-Mode Input Voltage		-350	-	2850	mV	

Receiver Electrical Characteristics

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
Output Differential Impedance	Z_O	90	100	110	Ω	
Differential Data Output Swing	$V_{OUT, P-P}$	-	-	900	mVP-P	1

Dual Function Signals

Parameter	Symbol	Min.	Typical	Max.	Unit	Notes
INT/RSTn	V_INT/RSTn_1	0.000	0.000	1.000	V	2
	V_INT/RSTn_2	0.000	0.000	1.000	V	3
	V_INT/RSTn_3	1.500	1.900	2.250	V	4
	V_INT/RSTn_4	2.750	3.000	3.465	V	5
LPWn/PRSn	V_ LPWn/PRSn_1	0.000	0.950	1.100	V	6
	V_ LPWn/PRSn _2	1.400	1.700	2.250	V	7
	V_ LPWn/PRSn _3	2.750	3.300	3.465	V	8

Notes:
1. Internally AC coupled, but requires an external 100Ω differential load termination.
2. INT/RSTn voltage for no module.
3. INT/RSTn voltage for module installed, H_RSTn=Low.
4. INT/RSTn voltage for module installed, H_RSTn=High, M_INT=Low.
5. INT/RSTn voltage for module installed, H_RSTn=High, M_INT= High.
6. LPWn/PRSn voltage for module installed, H_LPWn=Low.
7. LPWn/PRSn voltage for module installed, H_LPWn =High.
8. LPWn/PRSn voltage for no module.

Transmitter Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Lane Wavelengths	ก	1304.5	1311	1317.5	nm	1
Side-mode Suppression Ratio	SMSR	30	-	-	dB	5
Average Launch Power, each lane	P_0 (100G)	-2.9	-	4	dBm	2
	P_0 (50G)	-5.1	-	3	dBm	2
Outer Optical Modulation Amplitude, each lane	P_1 (100G)	-0.8		4.2	dBm	2
	P_1 (50G)	-3		2.8	dBm	2
Transmitter and Dispersion Penalty Eye Closure for 100Gbps PAM4, each lane	TDECQ 1	-	-	3.4	dB	3
Transmitter and Dispersion Penalty Eye Closure for 50Gbps PAM4, each lane	TDECQ 2	-	-	3.2	dB	4
Launch Power in OMA_{outer} Minus TDECQ for 100Gbps PAM4, each lane	OMA-TDECQ1	-2.2	-	-	dBm	3
Launch Power in OMA_{outer} Minus TDECQ for 50Gbps PAM4, each lane	OMA-TDECQ2	-4.4	-	-	dBm	4
Extinction Ratio	ER	3.5	-	-	dB	3,4
Average Launch Power of OFF Transmitter	P_{off}	-15	dBm			
Optical Return Loss Tolerance	ORLT	21.4	dB			
Transmitter reflectance		-26	dB			

Note:
1. 13nm width
2. Class 1 laser safety per FDA/CDRH and EN (IEC) 60825 regulations.
3. 106.25Gbps PAM4.
4. 53.125Gbps PAM4.
5. Modulated

Receiver Optical Characteristics

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Notes
Lane Wavelengths	ก	1304.5	1311	1317.5	nm	
100G Receiver Sensitivity (OMA)	RxSENS			-3.9	dBm	1
50G Receiver Sensitivity (OMA)	RxSENS			-6.1		2
Receiver Overload, each lane (P_{avg})	P_{OL}	4		-	dBm	
Damage Threshold, each lane		5		-	dBm	
Receive Power, each lane (OMA_{outer})	OMA	-		4.2	dBm	
Receiver Reflectance				-26	dB	
LOS De-Assert	LOSD			-10	dBm	
LOS Assert	LOSA	-16			dBm	
LOS Hysteresis		0.5			dBm	

Notes:
1. Measured with PRBS31Q test pattern, 53.125GBd, PAM4, BER<2.4E-4.
2. Measured with PRBS31Q test pattern, 26.2525GBd, PAM4, BER<2.4E-4.

Electrical Pin Description

Pin	Name	Function/Description	Logic	Direction	Plug Sequence	Notes
1	GND	Ground			1	
2	TX2p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
3	TX2n	Transmitter Data Inverted	CML-I	Input from Host	3	
4	GND	Ground			1	
5	TX4p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
6	TX4n	Transmitter Data Inverted	CML-I	Input from Host	3	
7	GND	Ground			1	
8	TX6p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
9	TX6n	Transmitter Data Inverted	CML-I	Input from Host	3	
10	GND	Ground			1	
11	TX8p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
12	TX8n	Transmitter Data Inverted	CML-I	Input from Host	3	
13	GND	Ground			1	
14	SCL	2-Wire Serial Interface Clock	LVCMOS-I/O	Bi-directional	3	1
15	VCC	+3.3 V Power		Power from Host	2	
16	VCC	+3.3 V Power		Power from Host	2	
17	LPWn/PRSn	Low-Power Mode/Module Present	Multi-Level	Bi-directional	3	2
18	GND	Ground			1	
19	RX7n	Receiver Data Inverted	CML-O	Output to Host	3	
20	RX7p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
21	GND	Ground			1	
22	RX5n	Receiver Data Inverted	CML-O	Output to Host	3	
23	RX5p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
24	GND	Ground			1	
25	RX3n	Receiver Data Inverted	CML-O	Output to Host	3	
26	RX3p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
27	GND	Ground			1	
28	RX1n	Receiver Data Inverted	CML-O	Output to Host	3	
29	RX1p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
30	GND	Ground			1	

Electrical Pin Description

Pin	Name	Function/Description	Logic	Direction	Plug Sequence	Notes
31	GND	Ground			1	
32	RX2p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
33	RX2n	Receiver Data Inverted	CML-O	Output to Host	3	
34	GND	Ground			1	
35	RX4p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
36	RX4n	Receiver Data Inverted	CML-O	Output to Host	3	
37	GND	Ground			1	
38	RX6p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
39	RX6n	Receiver Data Inverted	CML-O	Output to Host	3	
40	GND	Ground			1	
41	RX8p	Receiver Data Non-Inverted	CML-O	Output to Host	3	
42	RX8n	Receiver Data Inverted	CML-O	Output to Host	3	
43	GND	Ground			1	
44	INT/RSTn	Module Interrupt / Module Reset	Multi-Level	Bi-directional	3	2
45	VCC	+3.3 V Power		Power from Host	2	
46	VCC	+3.3 V Power		Power from Host	2	
47	SDA	2-Wire Serial Interface Data	LVCMOS-I/O	Bi-directional	3	1
48	GND	Ground			1	
49	TX7n	Transmitter Data Inverted	CML-I	Input from Host	3	
50	TX7p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
51	GND	Ground			1	
52	TX5n	Transmitter Data Inverted	CML-I	Input from Host	3	
53	TX5p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
54	GND	Ground			1	
55	TX3n	Transmitter Data Inverted	CML-I	Input from Host	3	
56	TX3p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
57	GND	Ground			1	
58	TX1n	Transmitter Data Inverted	CML-I	Input from Host	3	
59	TX1p	Transmitter Data Non-Inverted	CML-I	Input from Host	3	
60	GND	Ground			1	

Edge-corE NETWORKS

Top Side

60	GND	
59	Tx1p	
58	Tx1n	
57	GND	
56	Tx3p	
55	Tx3n	
54	GND	
53	Tx5p	
52	Tx5n	
51	GND	
50	Tx7p	
49	Tx7n	
48	GND	
47	SDA	
46	VCC	
45	VCC	
44	INT/SRTn	
43	GND	
42	Rx8n	
41	Rx8p	
40	GND	
39	Rx6n	
38	Rx6p	
37	GND	
36	Rx4n	
35	Rx4p	
34	GND	
33	Rx2n	
32	Rx2p	
31	GND	

Module Card Edge

Bottom Side

GND	1	
Tx2p	2	
Tx2n	3	
GND	4	
Tx4p	5	
Tx4n	6	
GND	7	
Tx6p	8	
Tx6n	9	
GND	10	
Tx8p	11	
Tx8n	12	
GND	13	
SCL	14	
VCC	15	
VCC	16	
LPWn/PRSn	17	
GND	18	
Rx7n	19	
Rx7p	20	
GND	21	
Rx5n	22	
Rx5p	23	
GND	24	
Rx3n	25	
Rx3p	26	
GND	27	
Rx1n	28	
Rx1p	29	
GND	30	

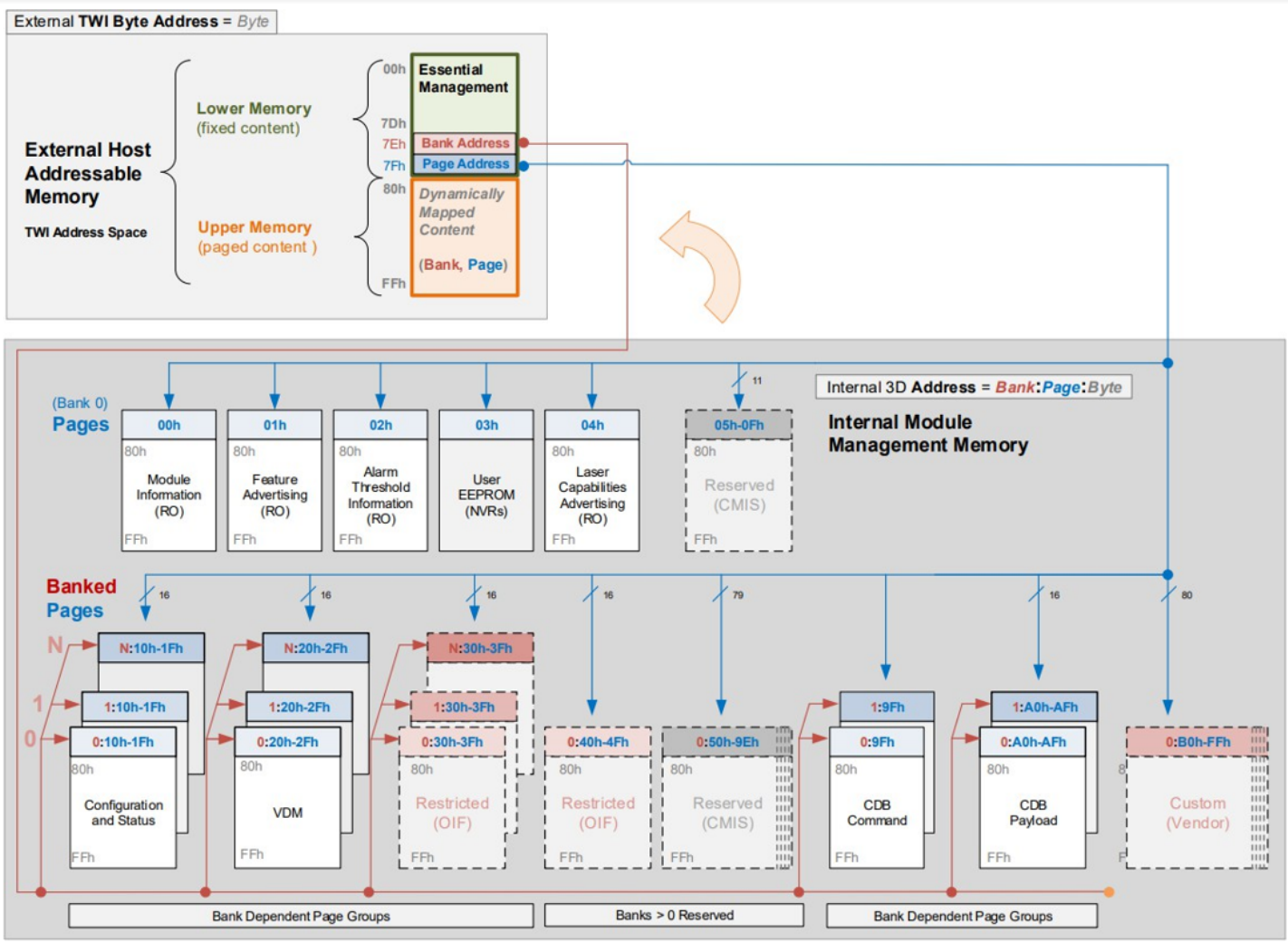
viewed from top

viewed from bottom

Notes:
1. Open-Drain with pull-up resistor on host.
2. See pin description of OSFP MSA for required circuit.

Digital Diagnostic Memory Map

Digital Diagnostics Monitoring is available on all OSFP products. A 2-wire serial interface provides users access to the module with a high clock frequency up to 100 KHz. The control interface and memory map of the OSFP modules are compliant with CMIS (Common Management Interface Specification) for pluggable transceivers. The memory space is arranged into a lower 128 bytes page and multiple upper space pages.



EEPROM Serial ID Memory Contents

CMIS transceivers define the lower 128 bytes of the two-wire serial bus address space for access to a variety of measurements and diagnostic functions, a set of control functions, and a means to select which of the various upper memory map pages are accessed on subsequent accesses. This portion of the address space is always directly addressable and thus is chosen for monitoring and control functions that may need to be repeatedly accessed. The lower page is subdivided into several areas as illustrated.

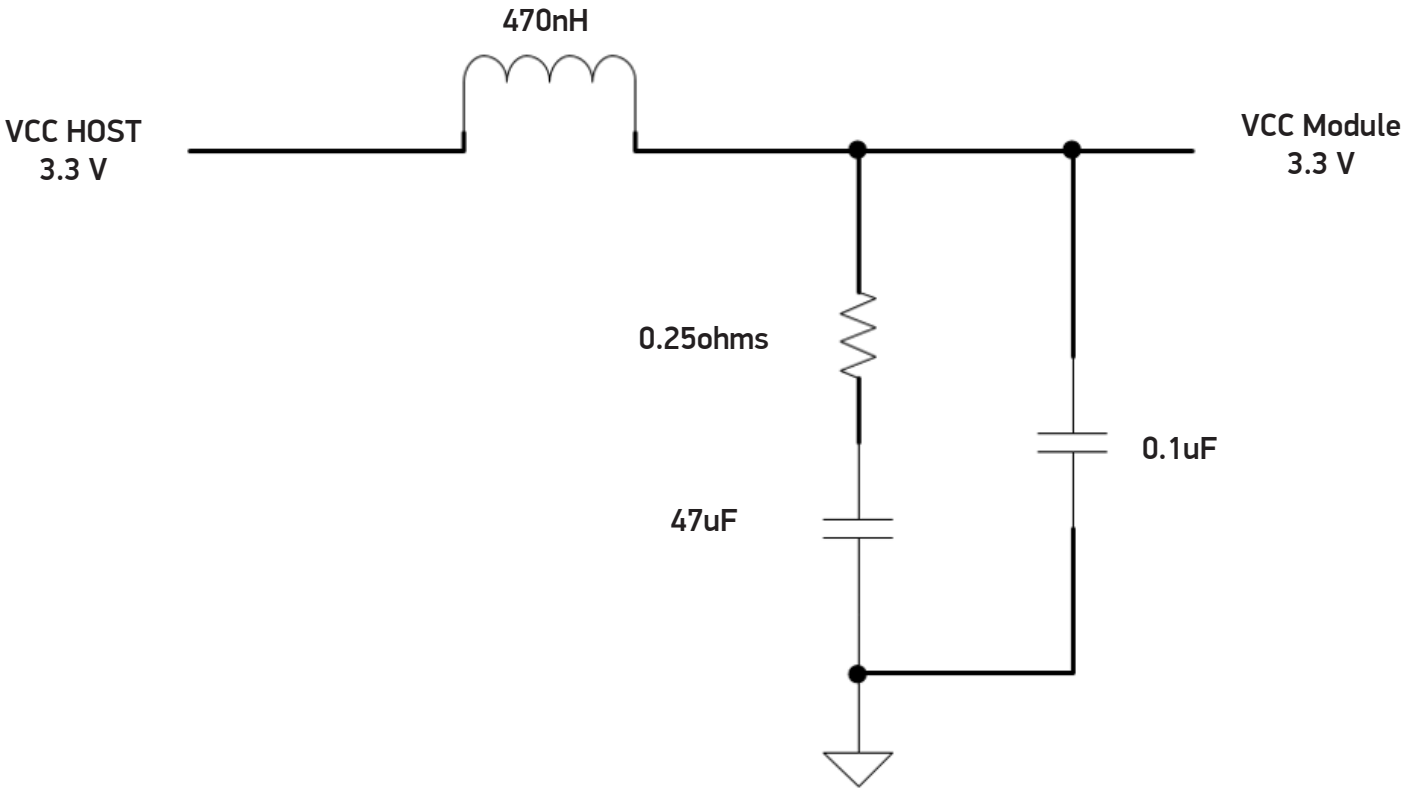
Address	Size	Subject Area	Description
0-2	3	Management Characteristics	Basic information about how this module is managed
3	1	Global Status Information	Current state of module, interrupt signal status
4-7	4	Flags Summary	Summary of flags set on specific pages (and banks)
8-13	6	Module-Level Flags	Flags that are not lane or data path specific
14-25	12	Module-Level Monitors	Monitors that are not lane or data path specific
26-30	5	Module-Level Controls	Controls applicable to the module as a whole
31-36	6	Module-Level Masks	Mask bits for the Module-Level Flags
37-38	2	CDB Command Status	Status of current CDB command
39-40	2	Module Active Firmware Version	Module Active Firmware Version number
41	1	Fault Information	Fault cause for entering module fault state
42-63	22	-	Reserved[22]
64-84	21	-	Custom[21]
85-117	33	Supported Applications Advertising	Applications supported by module data path(s)
118-125	8	Password Facilities	Password entry and change (mechanism only)
126-127	2	Page Mapping	Page mapping into host addressable upper memory

Data Address	Name of Field	Contents (Hex)	Description
128	Identifier	19	OSFP
129-144	Vendor Name	45 64 67 65 63 6F 72 65 20 20 20 20 20 20 20 20	Edgecore (ASCII)
145-147	Vendor OUI	3C 2C 99	-
148-163	Vendor PN	45 54 38 30 30 31 2D 32 44 52 34 20 20 20 20 20	“ET8001-2DR4” (ASCII)
164-165	Vendor REV	31 30	1.0(ASCII)
166-181	Vendor SN	32 33 32 38 31 30 30 30 30 31 20 20 20 20 20 20	“2328100001”
182-189	Date Code	32 33 30 31 31 36 20 20	Year (2 bytes), Month (2 bytes), Day (2 bytes) “230616”
190-199	CLEI Code		-
200-201	Module Power Characteristics	C0 38	Power class 7, 14W Maximum
202	Cable Assembly Link Length	00	
203	Connector Type	0C	MPO 1x12
204-209	Copper Cable Attenuation	00 00 00 00 00 00	-
210	Media Lane Information	00	
211	Cable Assembly Information	00	
212	Media Interface Technology	06	1310nm EML
213-220	Reserved	00	
221	Custom	00	
222	Checksum	xx	
223-255	Custom Info NV	00	

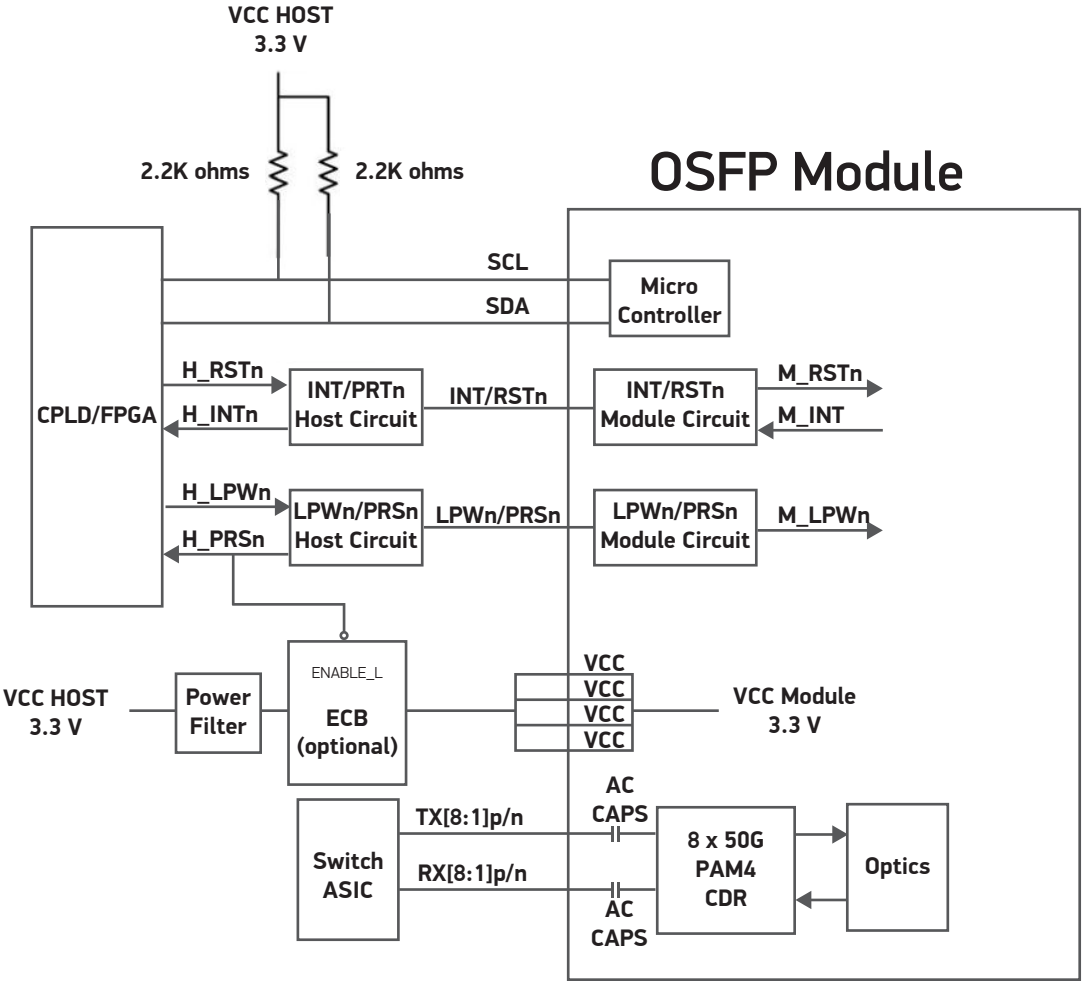
Note:

1. The “xx” byte should be filled in according to practical case. For more information, please refer to the related document of CMIS transceivers.

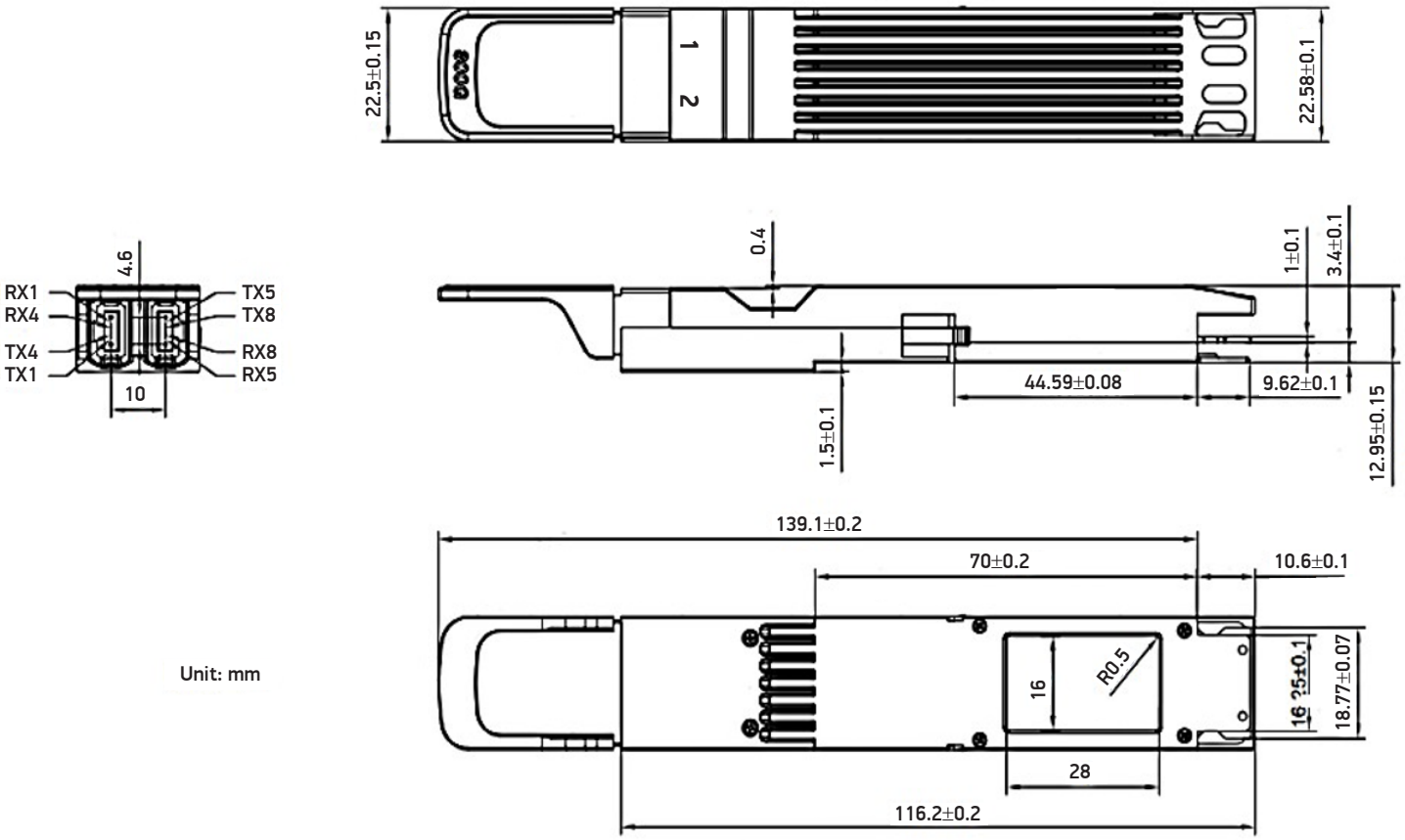
Recommended Host Board Power Supply Filter Network



Recommended Application Interface Block Diagram



Mechanical Specifications



Unit: mm

Warranty
Please check www.edge-core.com for the warranty terms in your country.

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